CIRCUIT CELLAR ONLINE

FEATURE ARTICLE

# High-Temperature Electronic Design

## Part 1: What Are Your Options?

**George Novacek**

Design options for temperatures beyond 125°C have been scarce in the past, but this month George shows us that there are ways to get around the technical problems and risk and still create state-of-the-art designs. Electronics from the common to the complex can benefit from finding new alternatives geared for elevated temperatures. If you're successful, the result could be simpler designs that are more robust, economical, and reliable.

In a recent article I wrote, "Thermal Considerations in Electronic Design" (*Circuit Cellar Online*, September 2000), I discussed several aspects of thermal management in electronic circuit design. I then recognized that specifications allow operation of the majority of semiconductor devices up to 85°C, with a handful reaching 125°C, and a few going as high as 170°C $T_{JMAX}$. That is usually the maximum junction temperature at zero power dissipation. When those devices' power dissipation is derated with the real loads in mind, the specification upper temperature limit becomes nothing more than the survival temperature.

For a long time it has been known that electronics, including the plain vanilla silicon devices available off the shelf, can operate well above the usually accepted maximum 125°C, but there remain considerable technical problems and, of course, risk. In this article, I'll look at state-of-the-art, high-temperature electronics and see what design options you have if operation at an elevated temperature is the preferred (or necessary) option.

Why would you want to operate at elevated, often way out of spec, temperatures? Because in harsh environments, systems inevitably consist of transducers, connected via long wires to their electronic controllers placed in more suitable locations. This results in increased electromagnetic and radio frequency interference susceptibility and a high level of measurement noise, numerous other design tradeoffs notwithstanding. Having to tailor system architecture to operate outside the controlled environment because of the electronic components' limitations often renders less than optimum designs. Consider a few examples where electronic systems are commonly used and their typical operating temperature ranges are well above the established upper limit.

In the automotive engine department, operating temperatures will routinely range between –40°C (–40°F) and 165°C (329°F). Components installed in wheels, such as those belonging to a braking system, will see the upper operating temperature hit a balmy 250°C (482°F), and the temperatures within the engine combustion chamber can reach as high as 1000°C (1832°F) without much effort. Aerospace components, such as those installed inside jet engines or "smart skins," may be routinely exposed between 300°C (572°F) and 600°C (1112°F). Even common industrial processes, nuclear reactor monitoring, or the humble consumer electronics found in places such as microwave ovens would benefit if they could operate inside zones where temperatures of hundreds of degrees are normal. Expect 250°C (482°F) in communications equipment, 500°C (932°F) in microwave ovens and 550°C (1022°F) in nuclear reactors.

If you could make electronics operate at those elevated temperatures, your designs would be simpler. With the electronics integrated within the controlled mechanical structures and without long wire interfaces and separate packaging, more robust, economical, and reliable operation could be achieved.

Are you concerned with operation at low temperatures? Probably not. Semiconductors will generally operate better at low temperatures, although you must make sure that circuits such as oscillators and switching power supplies start up even with the low-temperature-reduced gain. The reliability is significantly improved. Some devices, namely low-noise amplifiers, are cooled in specialized applications to reduce thermal noise. It is mainly the mechanics (such as packaging) and some passive devices (typically electrolytic capacitors) that present engineering challenges at low temperatures. However, if everything else fails, maintaining the internal temperature at some minimum level through the use of a heater is a fairly straightforward engineering task.

## A LITTLE THEORY

Before I can talk about the exotic technologies producing high-temperature semiconductors, let's take a good look at the ordinary, off-the-shelf silicon components and see what can be done with them. You will find that many can be pushed to operate reliably at surprising temperature levels, often exceeding 200°C. Unfortunately, manufacturers provide no data or support for exposing their components to the environment outside the specified limits. In fact, they discourage it. Although I sympathize with their attitude, this shouldn't stop us from generating the needed design data ourselves by test. Applying the results judiciously, you'll be able to achieve unprecedented environmental performance and leave the competition in the dust. But, you'll be on your own, so test, verify, and test again!

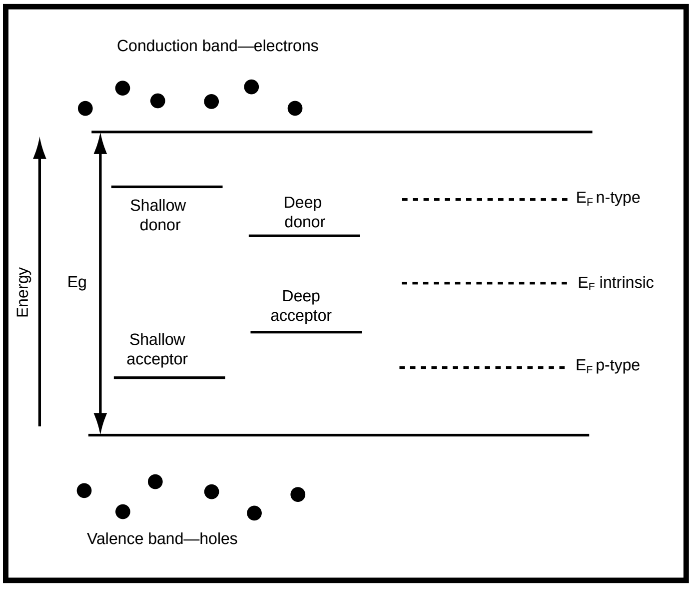

**Figure 1**—*Here you can see the relationship between the energy levels of the valence and the conduction bands, the deep and shallow donor and acceptor levels, and the Fermi levels of N-type, intrinsic, and P-type semiconductors.*

To understand the operation of semiconductors, consider Figure 1. In crystalline solids, electrons populate energy bands, which are separated by energy bandgaps. In this model, a full-valence band separated from a conduction band by a large bandgap characterizes an insulator. All of the electrons are tightly bound in chemical bonds.

Many electron volts (eV) of energy would be required to free the electrons, move them across the band, and thus, make the electric current flow. In a metal, the bandgap is either small or zero, and not all the electrons are tightly bound by the chemical bonds, so they are free to move in the conduction band. On the other hand, in a semiconductor, the bandgap is larger but still fairly small (about 1 to 3 eV). Consequently, the electrons can be thermally excited from the valence band to the conduction band, or introduced into the conduction band by doping the semiconductor with impurities.

## SIZE AND TYPE

The size and the type of the bandgap (direct versus indirect) plays a crucial role in the thermal performance of semiconductors. The leakage caused by the thermal excitation of the electrons is the most important limiting factor and the most common cause of failure during high-temperature operation. A quick review of some semiconductor materials, their respective bandgaps at room temperature, and associated temperatures for standardized leakage of 0.1 A/cm$^2$ can be seen in Table 1.

The bandgap is also affected by temperature. Figure 2 shows two common semiconductors—silicon and gallium arsenide.

The electrical characteristics of solid-state devices are also dependent on dopants, the impurities purposely introduced into the semiconductor during manufacturing. At high temperatures, the effects of the dopants tend to be swamped by the intrinsic carrier density, determined by the bandgap. Thus, devices with larger bandgap appear to have an advantage, but it is not that simple. There is the penalty of the larger forward voltage drop associated with larger bandgap, leading to larger internal power dissipation and, consequently, higher operating junction temperature. The forward voltage drop of a PN junction will decrease linearly with temperature, at the rate of approximately 2 mV/°C, decreasing power dissipation accordingly. The reverse leakage, however, will increase more than exponentially with temperature, and at one point, become dominant and potentially lead to thermal runaway. The larger bandgap generally means lower leakage, but unfortunately, there is also the leakage dependence on the direct/indirect type of bandgap. So, the result is that similar thermal performance can be expected from Si with 1.1 eV indirect bandgap as from GaAs with 1.3 eV direct bandgap.

## SILICON BIPOLAR TRANSISTORS

Let's review how an ordinary, off-the-shelf silicon bipolar transistor works. Figure 3 is a simplified diagram of a PNP

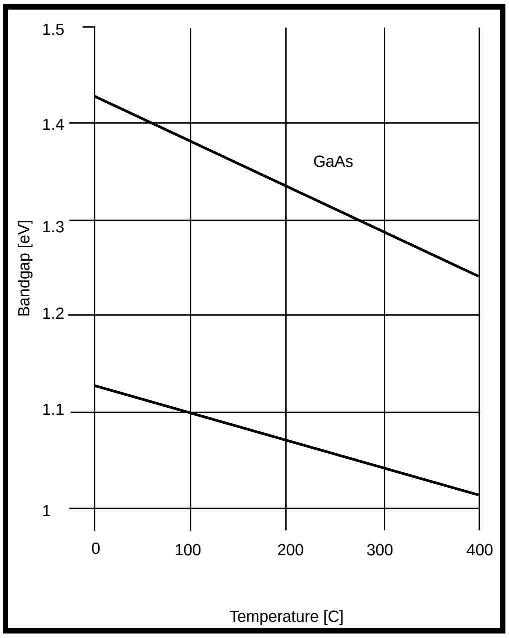

**Figure 2—***Here you can see the emperature dependence of bandgap energy in silicon (Si) and gallium arsenide (GaAs).*

transistor. (The NPN device can be understood by simply reversing junction polarities and interchanging the roles of electrons and holes.)

The transistor comprises a $p^+$-doped emitter and collector, separated by a thin n-conductor base. The base-emitter junction is forward biased, and the base-collector junction is reverse biased. The forward bias drives a large hole current into the base from the emitter. Because the base is thin, all but a fraction of the hole current reaches the base-collector depletion region. Many holes are collected in the collector as a result of the reverse base-collector battery potential. Therefore, $I_e$ » $I_c$, although only a fraction of the holes recombine with the electrons in the base, causing base current $I_{be}$. A second current component supplied into the base is the thermal leakage $I_{oc}$ of the reverse collector-base junction.

Analysis of this simple model points to four major temperature dependencies of the transistor characteristics. First, because the electron recombination time is temperature-dependent, the forward current gain will increase with temperature. Second, $I_c$ dependence on $V_{be}$ is also a function of temperature. Third, the reverse leakage current $I_{cb}$ increases with temperature and may affect the base bias point. And finally, the resistivity of silicon is itself temperature-dependent. These dependencies affect all the operational characteristics of the bipolar transistor and are mostly apparent in the design of analog circuits.

A quad op-amp usable from 0° to 300°C was built some years ago, but special layouts and processes to minimize leakage had to be used. The lower temperature operating point was not driven by the potential failure of the semiconductor but by the ability to compensate for the temperature effects. Extending compensation of the leakage effects, which varied between five orders of magnitude even with the special care taken in the chip design, was no easy task. With the emphasis on the high-temperature operation, the designers decided to limit the low temperature range. Overall, you have to assume that analog bipolar circuits operating at elevated temperatures are a rare breed.

However, with extensive tests, standard TTL circuits were found to operate reliably at 250°C. An accompanying problem was lower switching speed, lower noise margin, and lower output fan-out. Tests showed that the failures were caused by a decrease in the high-level output voltage, so although the circuit still toggled, its output was out of tolerance to drive a next TTL input. Dielectric isolated TTL integrated circuits suffered similar performance degradation but worked all the way up to 325°C.

## SILICON MOSFETS

MOSFETs (metal oxide semiconductor field effect transistors) are presently the most widely used transistors, whether as individual N- or P-channel devices or as CMOS (complementary metal oxide semiconductor) devices, using both N- and P-channel enhancement transistors.

Figure 4 shows a simplified diagram of an N- and P-channel transistor on a single, lightly doped P-type substrate. Source and drain electrodes are implanted into the substrate. Typically, the source is tied to the low potential, with the N drain positive and P drain negative. A silicon dioxide gate oxide is grown over the surface of the silicon between the gate and the drain. A metal gate electrode is deposited on top of the gate oxide, so the gate (with the gate oxide and silicon substrate) forms a capacitor. A positive (negative for P-channel) charge on the gate draws electrons to the surface of the silicon. When a threshold gate voltage ($V_{GTH}$) is exceeded, an N-type (P-type, respectively) channel between the source and drain is formed, and a current between the drain and source can flow. The conductance of the channel is controlled by the voltage applied to the gate.

P-channel MOSFETs operate in a manner similar to N-channel, with the doping, gate, and drain polarities reversed. In CMOS integrated circuits, however, where both N- and P-channel devices must be on the same substrate, one transistor is placed in a well of the appropriate polarity (see Figure 4). The substrate is normally grounded, although a bias may be applied.

Depletion MOSFETs have electrical characteristics similar to vacuum tubes. The channel current must be turned off by applying a voltage, and is achieved by lightly doping the channel and having the gate potential force the carriers out. In this article, I am only concerned with the thermal effects on

| Material | Electron voltage | Temperature |
|---|---|---|
| Silicon (Si) | 1.1 eV | 250°C |
| Gallium arsenide (GaAs) | 1.3 eV | 350°C |
| Gallium phosphide (GaP) | 2.34 eV | 550°C |
| Silicon carbide (SiC) | 2.9 eV | 900°C |
| Diamond | 5.5 eV | – |

**Table 1—***Here you can see the most common semiconductor materials with their bandgap and the corresponding maximum operating temperature.*

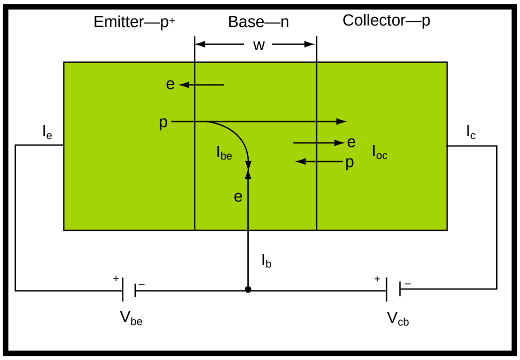

**Figure 3**—*Here is a PNP transistor in the normal operating mode, showing the principal current components. The width of the base region is shown as w.*

the MOSFET operation, so I'll not dwell on the intricacies of the MOSFET's inner workings.

Like bipolar transistors, unipolar transistors suffer from leakage. The leakage currents (see Figure 4) grow exponentially with temperature and can eventually become so large that the drain current is no longer practically controlled by the gate voltage. The threshold voltage ($V_{GTH}$) is typically defined as the gate voltage for which $I_D = 1\%$ of the drain saturation current. The $V_{GTH}$ shows a significant decrease in temperature (about –10 mV/°C), which means that at a high enough temperature the device may become permanently turned on. Although the leakage current increases with temperature, the saturation current and transconductance (i.e., gain) decrease dramatically.

An interesting and important characteristic of a MOSFET is an operating point where a zero temperature coefficient exists. Such a point (approximately $V_{GS} = 5$ V for Motorola's 2N4351) is crucial for analog operation over a wide temperature range. At that bias, $I_D$ is independent of temperature up to about 300°C.

Commercial MOS devices have been successfully used at temperatures significantly greater than 125°C. Common variety CMOS integrated circuits are functional to about 160°C, although switching speed reduction must be expected. Dielectric isolated devices are often functional at 200°C, and specially designed SOIs (silicon-on-insulators) function above 300°C. Even 500°C operation has been reported.

## SIX OF ONE...

As you've already seen, the fundamental limitation of silicon semiconductors is the excessive generation of carriers by thermal energy, in other words, leakage. At a sufficient temperature, thermally generated carriers can exceed doping levels until the device is no longer operative. For silicon-based semiconductors, the practically achievable temperature limit is near 400°C; the theoretical limit is somewhat higher. Nothing in life is free, so although a tradeoff exists in increasing of doping levels, thereby decreasing the leakage, the price to pay is a decreased breakdown voltage of the device.

One potential method of decreasing the leakage is by using a higher bandgap material, such as SiC, diamond, or GaAs. Another way is by reducing the junction area. An effective way of doing this is by SOI technology. Figure 5 shows a leakage comparison between regular silicon and an SOI device. Leakage reduction of SOI devices at high temperatures can be two to four orders of magnitude below silicon. SOI devices have been routinely operated at 300°C and as high as 500°C.

## SOI TECHNOLOGY

The SOI wafer is similar to the bulk MOSFET, but it also comprises a thin silicon layer over a thick buried oxide (BOX) on a bulk silicon substrate. Looking at Figure 4, you can envision it as small junction areas similar to the structure of the P-channel device located within the BOX, as opposed to the substrate. Figure 6 shows the actual cross section of the bulk and SOI devices for comparison. The substrate is now at the bottom side of the BOX. The result is a greatly reduced junction area with all its benefits.

The available SOI devices have been mostly optimized for 300°C operation. Their original application was for the radiation hardened devices, which also require the smaller junction area. High-temperature operation came as a fringe benefit. Another benefit of the smaller junction area is that the junction capacitance has been significantly reduced, and therefore, power consumption has decreased. The SOI technology has extended to analog devices, too. Operational amplifiers built with SOI devices have successfully passed tests for 1000 h of operation at 300°C.

Although the silicon-based technologies do not give us the great results that exotic ones do, their major advantage is that they can be used with the existing wafer manufacturing equipment worth billions of dollars worldwide. Until a similar industrial base is developed for the new technologies, they will, by necessity, play second fiddle.

## OTHER OPERATION PROBLEMS

Bringing the electrical characteristics of semiconductors, particularly leakage, under control is only a partial solution to the problem. Metal electromigration, metallization, and corrosion become critical concerns and, if not properly addressed, result in drastic reduction of reliability. Electromigration and corrosion are the major factors limiting the life of conductors and electrical contacts operating at elevated temperatures.

Packaging integrity is another serious concern, as

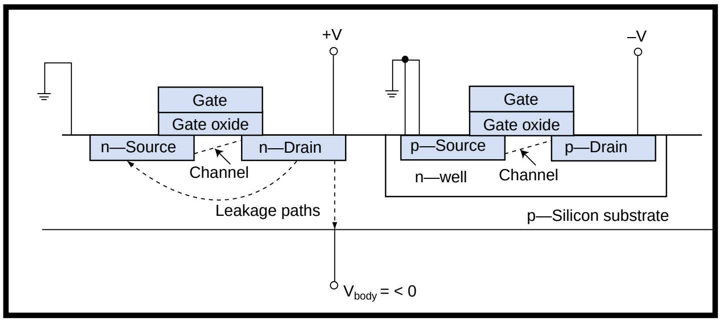

**Figure 4**—*Here is a simplified diagram of N- and P-channel MOSFETs on a P-type silicon wafer. Leakage paths between reverse-biased junctions are shown with dotted lines.*

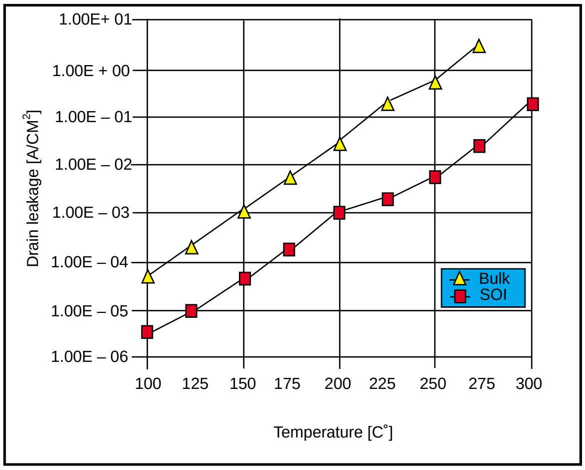

**Figure 5—***Leakage current versus temperature in SOI devices is at least two orders of magnitude lower than in the corresponding bulk MOSFETs.*

the present day packaging plastics begin to disintegrate after the temperature exceeds about 200°C. To date, metal encapsulation remains the only viable alternative for high-temperature devices.

Of paramount importance is the resistivity of the internal IC connections, because it directly affects the speed, power loss, and local heating effects. It is important to note that only the third and fourth lowest resistivity metals (gold, Au –2.35 x $10^{-8}$ ohm/m and aluminum, Al –2.653 x $10^{-8}$ ohm/m) have been used as thin films in large-scale integrated circuits manufacturing. Copper (Cu), with its resistivity of 1.63 x $10^{-8}$ ohm/m, rates in second place, having the benefit of 42% improvement over the conductivity of aluminum. Copper is difficult to use in silicon fabrication, but great strides have already been made in using it in silicon-based ICs. Intel's Coppermine series is a good example, but aluminum and gold still hold the lead. The highest conductivity metal (silver, Ag, with 1.59 x $10^{-8}$ ohm/m) seems to be too difficult to match with the current silicon IC fabrication process.

I've discussed quite a bit in this first part, and because I've already covered internal IC connections, next month I'll go into soldering, wire insulation, and so forth. They are concerns for successful high-temperature operation. I'd also like to take a look at passive components. So, join me next month, and I'll pick up where I left off.

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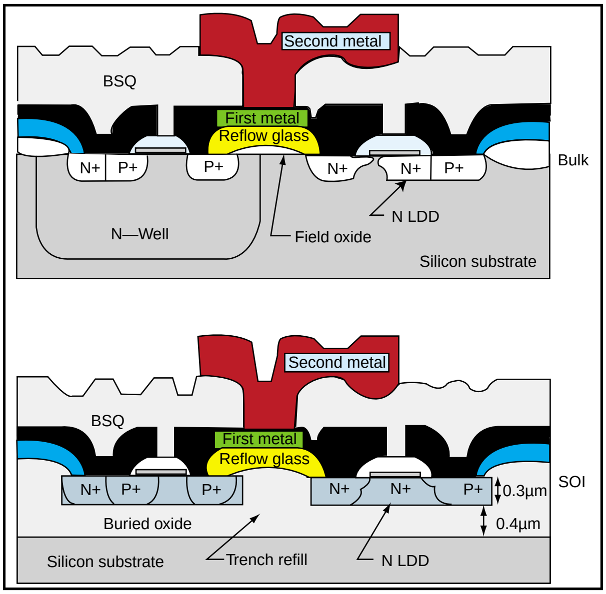

**Figure 6—***The actual cross section of SOI and bulk type MOSFETs can be seen here.*

## SOURCES

**2N4351**
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**Coppermine series**
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